Deval Shah

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RESEARCH INTERESTS

Computer architecture, Autonomous robotics, Machine learning

EDUCATION

University of British Columbia **2018-2023** (expected)
Ph.D. candidate (Department of Electrical and Computer Engineering)
Supervisor: Tor M. Aamodt
Research: Energy-Efficient Acceleration for Autonomous Robotics
Awards: Four Year Doctoral Fellowship (4YF), UBC Presidential Excellence Award

Indian Institute of Technology, Bombay **2014-2017**
Master of Technology (Department of Electrical Engineering) (CGPA: 9.98/10)
Specialization: Microelectronics and VLSI Engineering
Thesis: Lightweight Forth Programmable NoCs
Awards: Best Master Thesis, Silver medal for 1st rank in the department

Maharaja Sayajirao University of Baroda, India **2010-2014**
Bachelor of Engineering (Department of Electrical Engineering) (GPA: 4/4)
Specialization: Electronics and Instrumentation
Project: Design and implementation of automated inventory management system
Awards: 1st rank in the Faculty of Technology among 1100 students

WORK EXPERIENCE

Qualcomm India Pvt. Ltd., Bangalore **2017-2018**
Engineer, Design Technology and Methodology
• Worked on timing closure methodologies, clock convergence, and Power Performance Area (PPA) optimization.
• Built wrappers in Tcl/Tk around different tools such as Synopsis Primetime, Design Compiler, and Tweaker to develop a customized flow for engineering change order (ECO) convergence.
• Awarded QualStar for outstanding contributions to design analysis for timing closure.

RESEARCH PROJECTS

• **Hardware accelerator** design to enable **real-time motion planning** for robotic manipulators with algorithm-hardware co-optimization of learning-based motion planning approaches. Built **microarchitecture simulator** and **Verilog model** for the proposed accelerator. (**ISCA 2023**)

• **Binary-encoded labels** for **deep regression networks**. Studied the design space of binary-encoded labels for regression tasks to demonstrate its potential using manually designed encoding functions and motivate problem-specific exploration of the design space. The second phase of the project focused on automatically learning binary-encoded labels for a given problem. Evaluated the proposed approach on complex regression tasks, including **headpose estimation, facial landmark detection, age estimation, and autonomous driving.** **(ICLR 2022 Spotlight, ICLR 2023 Spotlight)**

• Characterizing and improving the **soft-error resilience** of **motion planning accelerators** for **autonomous robots**. Proposed a reliability metric for motion planning accelerators to facilitate faster **fault characterization** and cost-effective **error mitigation**. Developed microarchitecture simulators and Verilog models of four existing motion planning accelerators for evaluation. **(TCPS 2023)**

• An **event-driven GPU execution model (EDGE)** that enables non-CPU devices to directly launch preconfigured tasks on a GPU without CPU interaction. The proposed execution model improves GPU support for latency-sensitive fine-grained streaming tasks and multi-programming. Evaluated the proposed approach using **Gem5-GPU**, a CPU-GPU system simulator. (**PACT 2019**)

• Performance analysis of machine learning workloads using a detailed GPU simulator. The project focused on **cuDNN** and **Pytorch** support for **GPGPU-Sim**, a widely used GPU simulator, to enable performance analysis of machine learning workloads. (**ISPASS 2018**)

• Performance analysis of **machine learning workloads** on deep neural network (DNN) accelerators using a **system simulator**. Worked on integrating **DNNSim** with **gem5**. Implemented a software layer using **NNAPI** to communicate with a hardware simulator (e.g., DNNSim) integrated with gem5.

• **ForthNoC**, a configurable **synthesizable NoC generator** with **programmable routers** built around lightweight **stack-based Forth cores**. ForthNoC supports features such as adaptive routing, broadcast/multicast, and systolic array computing that can be implemented through programming the routers. (**VLSID 2018**)

• Design and analysis of **GPU-based circuit simulator** based on Modified Nodal Analysis. **CULA** library with CUDA programming was used for the implementation.

• Designed and **synthesized** architecture of 2-wide fetch, 6-stage pipelined **superscalar processor** for ARMv7 equivalent ISA using **VHDL** and **Altera Quartus**. Studied different designs of major blocks, including branch predictors, reservation stations, and load queues.

RESEARCH PAPERS

• D. Shah, Z. Y. Xue, K. Pattabiraman, T. M. Aamodt, Characterizing and Improving Resilience of Accelerators to Memory Errors in Autonomous Robots, ACM Transactions on Cyber-Physical Systems, **TCPS 2023**
• D. Shah, N. Yang, T. M. Aamodt, Energy-efficient Realtime Motion Planning, International Symposium on Computer Architecture, **ISCA 2023**
• D. Shah, T. M. Aamodt, Learning Label Encodings for Deep Regression, International Conference on Learning Representations, **ICLR 2023** (**Selected for spotlight presentation**)
• D. Shah, Z. Y. Xue, T. M. Aamodt, Label Encoding for Regression Networks, International Conference on Learning Representations, **ICLR 2022** (**Selected for spotlight presentation**)
• T. H. Hetherington, M. Lubeznov, D. Shah, T M. Aamodt, EDGE: Event-Driven GPU Execution, Parallel Architectures and Compilation Techniques, **PACT 2019**
• J. Lew, D. Shah, S. Pati, S. Cattell, M. Zhang, A. Sandhupatla, C. Ng, N. Goli, M. D. Sinclair, T. G. Rogers, T. M. Aamodt, Analyzing Machine Learning Workloads Using a Detailed GPU Simulator, International Symposium on Performance Analysis of Systems and Software, **ISPASS 2018**
• V. B. Y. Kumar, D. Shah, M. Datar, S. Patkar, Lightweight Forth Programmable NoCs, International VLSI Design Embedded Systems conference, **VLSID 2018**

SCHOLASTIC ACHIEVEMENTS

• Awarded Four Year Fellowship during Ph.D. program. **2018-2022**
• Conferred with Silver medal for securing **1st rank** in Electrical department, IIT Bombay. **2017**
• Awarded "**Best Master's Thesis**", Electrical Department, IIT Bombay. **2017**
• Secured **all-India rank 105** in General Aptitude Test in Engineering among **2,16,365** candidates. **2014**
• Achieved **1st** rank among **90,683 students** in HSC exam conducted by Gujarat State Board. **2010**

TECHNICAL SKILLS

Programming Languages & Libraries: Verilog, VHDL, C/C++, Python, CUDA, PyTorch, TensorFlow, Open Motion Planning Library, Flexible Collision Library, BASH, OpenMP, MPI, systemC, TCL/TK

Open-source Simulators: GPGPU-Sim, Gem5, Gem5-GPU, Klampt Robotic Simulator

Tools: Synopsis Primetime and Design Compiler, Altera Quartus, OpenAI Gym, ModelSim, Xilinx ISE, Vivado HLS, GDB, Intel VTune profiler, Ngspice

PROFESSIONAL EXPERIENCE

Indian Institute of Technology Bombay, India **2014-2017**
System Administrator, Department of Electrical Engineering
• Maintained the department-wide email servers, storage servers, computing facilities, and network facilities.
• Built and maintained websites for the EE department and thesis database portal.

University of British Columbia **2018-2022**
Teaching Assistant, Department of Electrical and Computer Engineering
• Served as a teaching assistant for several courses, including Introduction to Microcomputers, Digital Systems Design, and Microcomputer Systems Design.

RELEVANT COURSES

- Compute Accelerator Architectures
- Computer Architecture
- Hardware Description Languages
- Machine Learning
- High Performance Scientific Computing
- Advanced Topics in Computer Architecture
- VLSI Design
- Advanced Machine Learning