Abdullah Giray Yağlıkçı

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Short Bio

I am a Ph.D. candidate in the Safari Research Group at ETH Zürich, working with Prof. Onur Mutlu. My current broader research interests are in reliable and high performance computer architecture, systems, and hardware security with a special focus on DRAM robustness and performance. In particular, my PhD research focuses on understanding and solving the read disturbance vulnerability of DRAM chips. I have published several works on this topic in major venues such as HPCA, MICRO, DSN, ISCA, and USENIX Security. One of these works, BlockHammer, was named as a finalist by Intel in 2021 for the Intel Hardware Security Academic Award. My RowHammer research is in part supported by Google and the Microsoft Swiss Joint Research Center.

Education

ETH Zürich		
Department of Information Technology and Electrical Engineering	- PhD	(2018-ongoing)
University of Notre Dame Du Lac		
Department of Computer Engineering	- MS	(2016)
TOBB University of Economics & Technology		
Department of Computer Engineering	- MS	(2014)
Department of Electrical Engineering	- BS	(2011)

First-Author Publications

- **A. Giray Yağlıkçı,** Minesh H. Patel, Jeremie S. Kim, Lois Orosa, Roknoddin Azizibarzoki, Hasan Hassan, Ataberk Olgun, Jisung Park, Konstantinos Kanellopoulos, Taha Shahroodi, Saugata Ghose, Onur Mutlu, *"BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows,"* in HPCA 2021. Slides: [PPT | PDF] Talk: [2mins] [22mins]
- **A. Giray Yağlıkçı,** Haocong Luo, Geraldo F. de Oliveira, Ataberk Olgun, Minesh Patel, Jisung Park, Hasan Hassan, Jeremie S. Kim, Lois Orosa, and Onur Mutlu, *"Understanding RowHammer Under Reduced Wordline Voltage: An Experimental Study Using Real DRAM Devices,"* in DSN, 2022. Slides: [PPT | PDF] Talk:[2mins][33mins]
- Lois Orosa*, **A. Giray Yaglikci*,** Haocong Luo, Ataberk Olgun, Jisung Park, Hasan Hassan, Minesh Patel, Jeremie S. Kim, and Onur Mutlu, *"A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses,"* in MICRO, 2021. Slides: [PPT | PDF] Talk: [21mins]
- **A. Giray Yağlıkçı**, Ataberk Olgun, Minesh Patel, Haocong Luo, Hasan Hassan, Lois Orosa, Oguz Ergin, and Onur Mutlu, *"HiRA: Hidden Row Activation for Reducing Refresh Latency of Off-the-Shelf DRAM Chips,"* in MICRO, 2022. Slides: [PPT | PDF] Talk: [15mins][36mins]

Major Co-Author Publications

- Ataberk Olgun, Yahya Can Tugrul, Nisa Bostanci, Ismail Emir Yuksel, Haocong Luo, Steve Rhyner, **A. Giray Yaglikci**, Geraldo F. Oliveira, and Onur Mutlu, "*ABACuS: All-Bank Activation Counters for Scalable and Low Overhead RowHammer Mitigation*," USENIX Security, 2024.
- Haocong Luo, Ataberk Olgun, **A. Giray Yaglikci**, Yahya Can Tugrul, Steve Rhyner, Meryem Banu Cavlak, Joël Lindegger, Mohammad Sadrosadati, and Onur Mutlu. "*RowPress: Amplifying Read Disturbance in Modern DRAM Chips*," in ISCA, 2023.
- Ataberk Olgun, Majd Osseiran, **A. Giray Yaglikci**, Yahya Can Tugrul, Haocong Luo, Steve Rhyner, Behzad Salami, Juan Gomez Luna, and Onur Mutlu, "*An Experimental Analysis of RowHammer in HBM2 DRAM Chips*," in DSN (Disrupt), 2023.

- Onur Mutlu, Ataberk Olgun, and **A. Giray Yaglikci**, *"Fundamentally Understanding and Solving RowHammer"* Invited Special Session Paper at ASP-DAC, 2023.
- Jawad Haj-Yahya, Jeremie S. Kim, **A. Giray Yaglikci,** Ivan Puddu, Lois Orosa, Juan Gomez Luna, Mohammed Alser, and Onur Mutlu, *"IChannels: Exploiting Current Management Mechanisms to Create Covert Channels in Modern Processors,"* ISCA, 2021.
- Jeremie S. Kim, Minesh Patel, **A. Giray Yaglikci**, Hasan Hassan, Roknoddin Azizi, Lois Orosa, and Onur Mutlu, *"Revisiting RowHammer: An Experimental Analysis of Modern Devices and Mitigation Techniques,"* in ISCA 2020.
- Jawad Haj-Yahya, M. Alser, J. Kim, **A. Giray Yaglikci**, N. Vijaykumar, E. Rotem, and O. Mutlu, *"SysScale: Exploiting Multi-domain Dynamic Voltage and Frequency Scaling for Energy Efficient Mobile Processors,"* in ISCA 2020.
- Saugata Ghose, **A. Giray Yaglikci**, Raghav Gupta, Donghyuk Lee, K. Kudrolli, William X. Liu, Hasan Hassan, Kevin K. Chang, Niladrish Chatterjee, Aditya Agrawal, Michael O'Connor, and Onur Mutlu, *"What Your DRAM Power Models Are Not Telling You: Lessons from a Detailed Experimental Study,"* in SIGMETRICS 2018.
- Kevin Chang, **A. Giray Yağlıkçı,** Saugata Ghose, Aditya Agrawal, Niladrish Chatterjee, Abishek Kashyap, Donghyuk Lee, Michael O'Connor, Hasan Hassan, and Onur Mutlu. *"Understanding Reduced-Voltage Operation in Modern DRAM Devices: Experimental Characterization, Analysis, and Mechanisms"*, SIGMETRICS, 2017

Talks and Lectures

- Memory Security, Reliability, Safety Problems and Solutions Lecture in ETHZ, 2023. Video: [3 hrs]
- Data Retention and Memory Refresh Lecture in ETHZ, 2023. Video: [3 hrs]
- Memory Latency Lecture in ETHZ, 2023. Video: [3 hrs]
- Fundamentally Understanding and Solving RowHammer in ASP-DAC, 2023. Video: [26 mins]
- Fundamentally Understanding and Solving RowHammer in AMLD, 2022. Video: [20 mins]

Service

- Reviewer for DSN'23, TODAES'22, ASPLOS AE'24 and IEEE CAL'23
- Student Assistant to the PC chairs for DSN'23
- Subreviewer for ASPLOS: 2018 and 2022; HPCA: 2018 and 2021; MICRO: 2017, and 2019-2023; DSN: 2017, 2019, 2020, and 2022; ISCA: 2017, 2019, 2020, and 2022; TCAD: 2019, 2021, and 2022

Employment

ETH Zurich **Scientific Assistant (Feb 2018 - ongoing)**
I am both a research and a teaching assistant in ETH Zurich. Please see above for the publication list.

Intel Labs **Research Intern (Aug 2017 - Feb 2018)**
I have analyzed the performance bottlenecks of computer vision applications at main memory level.

Carnegie Mellon University **Research Assistant (Aug 2016 - Jul 2017)**
I built the necessary infrastructure and conducted real-world experiments towards understanding latency and energy characteristics of DRAM chips. I heavily contributed to two papers: [Chang+ 2017] and [Ghose+ 2018].

University of Notre Dame Du Lac **Research Assistant (Aug 2014 - Aug 2016)**
Research project: Software-guided prefetching for graph applications.

TOBB University of Economics & Technology **Teaching/Research Assistant (Jan 2012 - Aug 2014)**
Research Project: Architecture design for an FPGA-based OpenCL Compatible Digital Signal Processing Accelerator

Kasırga Information Systems Ltd **Intern (Sep-Dec 2009), Engineer (May-Dec 2011)**
Project: An FPGA-based data acquisition hardware for mechanical balancing machines.

Yumruk Space and Defense Industry Ltd **Intern Electrical Engineer (May 2010 - Apr 2011)**
Project: Human motion detecting and alarming component: hardware, software, and embedded software designs.

Other Publications

- Ataberk Olgun, Hasan Hassan, **A Giray Yaglikci**, Yahya Can Tuƒürul, Lois Orosa, Haocong Luo, Minesh Patel, Oguz Ergin, Onur Mutlu, "DRAM Bender: An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips" IEEE TCAD, 2023.

- F. Nisa Bostanci, Ataberk Olgun, Lois Orosa, **A. Giray Yaglikci,** Jeremie S. Kim, Hasan Hassan, Oguz Ergin, and Onur Mutlu, *"DR-STRaNGe: End-to-End System Design for DRAM-based True Random Number Generators,"* HPCA, 2022.
- Jawad Haj Yahya, Jeremie S. Kim, **A. Giray Yaglikci,** Jisung Park, Efraim Rotem, Yanos Sazeides, and Onur Mutlu, *"DarkGates: A Hybrid Power-Gating Architecture to Mitigate the Performance Impact of Dark-Silicon in High Performance Processors,"* HPCA, 2022.
- Ataberk Olgun, Minesh Patel, **A. Giray Yaglikci**, Haocong Luo, Jeremie S. Kim, F. Nisa Bostanci, Nandita Vijaykumar, Oguz Ergin, and Onur Mutlu, *"QUAC-TRNG: High-Throughput True Random Number Generation Using Quadruple Row Activation in Commodity DRAM Chips,"* ISCA, 2021.
- Haocong Luo, Taha Shahroodi, Hasan Hassan, Minesh Patel, **A. Giray Yaglikci**, Lois Orosa, Jisung Park, and Onur Mutlu, *"CLR-DRAM: A Low-Cost DRAM Architecture Enabling Dynamic Capacity-Latency Trade-Off,"* in ISCA 2020.
- Skanda Koppula, Lois Orosa, **A. Giray Yaglikci,** Roknoddin Azizi, Taha Shahroodi, Konstantinos Kanellopoulos, and Onur Mutlu, *"EDEN: Energy-Efficient, High-Performance Neural Network Inference Using Approximate DRAM,"* in MICRO 2019.
- Hasan Hassan, Minesh Patel, Jeremie S. Kim, **A. Giray Yağlıkçı**, Nandita Vijaykumar, Nika Mansouri Ghiasi, Saugata Ghose, Onur Mutlu, *"CROW: A Low-Cost Substrate for Improving DRAM Performance, Energy Efficiency, and Reliability,"* in ISCA 2019.
- **A. Giray Yaglikci,** Jeremie S. Kim, Fabrice Devaux, and Onur Mutlu, *"Security Analysis of the Silver Bullet Technique for RowHammer Prevention,"* arXiv, 2021.

Communication Skills with Humans and Machines

- **Human Languages:** English (Professional), Turkish (Native), German (A1)
- **Preferred Hardware Description Language:** Verilog
- **Preferred Programming Languages:** C++, Python